ANALOG DEVICES

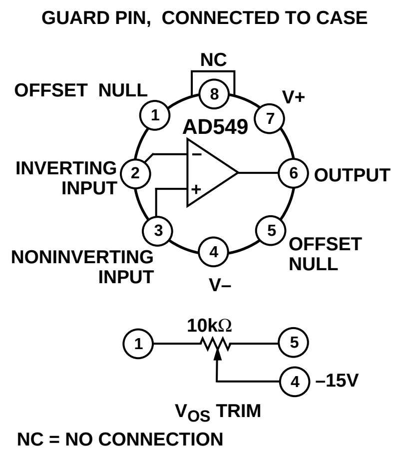
Ultralow Input Bias Current Operational Amplifier

AD549*

FEATURES
Ultralow Bias Current: 60 fA max (AD549L)
250 fA max (AD549J)
Input Bias Current Guaranteed Over Common-Mode Voltage Range
Low Offset Voltage: 0.25 mV max (AD549K)
1.00 mV max (AD549J)
Low Offset Drift: 5 μV/°C max (AD549K)
20 μV/°C max (AD549J)
Low Power: 700 μA max Supply Current
Low Input Voltage Noise: 4 μV p-p 0.1 Hz to 10 Hz
MIL-STD-883B Parts Available

APPLICATIONS
Electrometer Amplifiers
Photodiode Preamp
pH Electrode Buffer
Vacuum Ion Gage Measurement

CONNECTION DIAGRAM



PRODUCT DESCRIPTION

The AD549 is a monolithic electrometer operational amplifier with very low input bias current. Input offset voltage and input offset voltage drift are laser trimmed for precision performance. The AD549's ultralow input current is achieved with "Topgate" JFET technology, a process development exclusive to Analog Devices. This technology allows the fabrication of extremely low input current JFETs compatible with a standard junction-isolated bipolar process. The 10^{15} Ω common-mode impedance, a result of the bootstrapped input stage, insures that the input current is essentially independent of common-mode voltage.

The AD549 is suited for applications requiring very low input current and low input offset voltage. It excels as a preamp for a wide variety of current output transducers such as photodiodes, photomultiplier tubes, or oxygen sensors. The AD549 can also be used as a precision integrator or low droop sample and hold. The AD549 is pin compatible with standard FET and electrometer op amps, allowing designers to upgrade the performance of present systems at little additional cost.

The AD549 is available in a TO-99 hermetic package. The case is connected to Pin 8 so that the metal case can be independently connected to a point at the same potential as the input terminals, minimizing stray leakage to the case.

***Protected by Patent No. 4,639,683.**

The AD549 is available in four performance grades. The J, K, and L versions are rated over the commercial temperature range 0°C to +70°C. The S grade is specified over the military temperature range of –55°C to +125°C and is available processed to MIL-STD-883B, Rev C. Extended reliability PLUS screening is also available. Plus screening includes 168-hour burn-in, as well as other environmental and physical tests derived from MIL-STD-883B, Rev C.

PRODUCT HIGHLIGHTS

1. The AD549's input currents are specified, 100% tested and guaranteed after the device is warmed up. Input current is guaranteed over the entire common-mode input voltage range.
2. The AD549's input offset voltage and drift are laser trimmed to 0.25 mV and 5 μV/°C (AD549K), 1 mV and 20 μV/°C (AD549J).
3. A maximum quiescent supply current of 700 μA minimizes heating effects on input current and offset voltage.
4. AC specifications include 1 MHz unity gain bandwidth and 3 V/μs slew rate. Settling time for a 10 V input step is 5 μs to 0.01%.
5. The AD549 is an improved replacement for the AD515, OPA104, and 3528.

REV. A

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AD549–SPECIFICATIONS (@ +25°C and V_S = +15 V dc, unless otherwise noted)

Model	AD549J			AD549K			AD549L			AD549S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT BIAS CURRENT[1]													
Either Input, V_{CM} = 0 V		150	**250**		75	**100**		40	**60**		75	**100**	fA
Either Input, V_{CM} = ±10 V		150	250		75	100		40	60		75	100	fA
Either Input at T_{MAX}, V_{CM} = 0 V		11			4.2			2.8			420		pA
Offset Current		50			30			20			30		fA
Offset Current at T_{MAX}		2.2			1.3			0.85			125		pA
INPUT OFFSET VOLTAGE[2]													
Initial Offset		0.5	**1.0**		0.15	**0.25**		0.3	**0.5**		0.3	**0.5**	mV
Offset at T_{MAX}			**1.9**			**0.4**			**0.9**			**2.0**	mV
vs. Temperature		10	**20**		2	**5**		5	**10**		10	**15**	µV/°C
vs. Supply		32	**100**		10	**32**		10	**32**		10	**32**	µV/V
vs. Supply, T_{MIN} to T_{MAX}		32	**100**		10	**32**		10	**32**		32	**50**	µV/V
Long-Term Offset Stability		15			15			15			15		µV/Month
INPUT VOLTAGE NOISE													
f = 0.1 Hz to 10 Hz		4			4	**6**		4			4		µV p-p
f = 10 Hz		90			90			90			90		nV/√Hz
f = 100 Hz		60			60			60			60		nV/√Hz
f = 1 kHz		35			35			35			35		nV/√Hz
f = 10 kHz		35			35			35			35		nV/√Hz
INPUT CURRENT NOISE													
f = 0.1 Hz to 10 Hz		0.7			0.5			0.36			0.5		fA rms
f = 1 kHz		0.22			0.16			0.11			0.16		fA/√Hz
INPUT IMPEDANCE													
Differential V_{DIFF} = ±1		10^{13}‖1			10^{13}‖1			10^{13}‖1			10^{13}‖1		Ω‖pF
Common Mode V_{CM} = ±10		10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8			10^{15}‖0.8		Ω‖pF
OPEN-LOOP GAIN													
V_O @ ±10 V, R_L = 10 k	**300**	1000		**300**	1000		**300**	1000		**300**	1000		V/mV
V_O @ ±10 V, R_L = 10 k, T_{MIN} to T_{MAX}	**300**	800		**300**	800		**300**	800		**300**	800		V/mV
V_O = ±10 V, R_L = 2 k	**100**	250		**100**	250		**100**	250		**100**	250		V/mV
V_O = ±10 V, R_L = 2 k, T_{MIN} to T_{MAX}	**80**	200		**80**	200		**80**	200		**25**	150		V/mV
INPUT VOLTAGE RANGE													
Differential[3]			±20			±20			±20			±20	V
Common-Mode Voltage	**–10**		**+10**	**–10**		**+10**	**–10**		**+10**	**–10**		**+10**	V
Common-Mode Rejection Ratio													
V = +10 V, –10 V	**80**	90		**90**	100		**90**	100		**90**	100		dB
T_{MIN} to T_{MAX}	**76**	80		**80**	90		**80**	90		**80**	90		dB
OUTPUT CHARACTERISTICS													
Voltage @ R_L = 10 k, T_{MIN} to T_{MAX}	**–12**		**+12**	**–12**		**+12**	**–12**		**+12**	**–12**		**+12**	V
Voltage @ R_L = 2 k, T_{MIN} to T_{MAX}	**–10**		**+10**	**–10**		**+10**	**–10**		**+10**	**–10**		**+10**	V
Short Circuit Current	**15**	20	**35**	**15**	20	**35**	**15**	20	**35**	**15**	20	**35**	mA
T_{MIN} to T_{MAX}	**9**			**9**			**9**			**6**			mA
Load Capacitance Stability G = +1		4000			4000			4000			4000		pF
FREQUENCY RESPONSE													
Unity Gain, Small Signal	0.7	1.0		0.7	1.0		0.7	1.0		0.7	1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate	2	3		2	3		2	3		2	3		V/µs
Settling Time, 0.1%		4.5			4.5			4.5			4.5		µs
0.01%		5			5			5			5		µs
Overload Recovery, 50% Overdrive, G = –1		2			2			2			2		µs

Model	AD549J			AD549K			AD549L			AD549S			
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**		0.60	**0.70**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	–55		+125	°C
Storage	–65		+150	–65		+150	–65		+150	–65		+150	°C
PACKAGE OPTION													
TO-99 (H-08A)	AD549JH			AD549KH			AD549LH			AD549SH, AD549SH/883B			
Chips	AD549JChips												

NOTES
[1]Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. Bias current increases by a factor of 2.3 for every 10°C rise in temperature.
[2]Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[3]Defined as max continuous voltage between the inputs such that neither input exceeds ±10 V from ground.
Specifications subject to change without notice.
All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

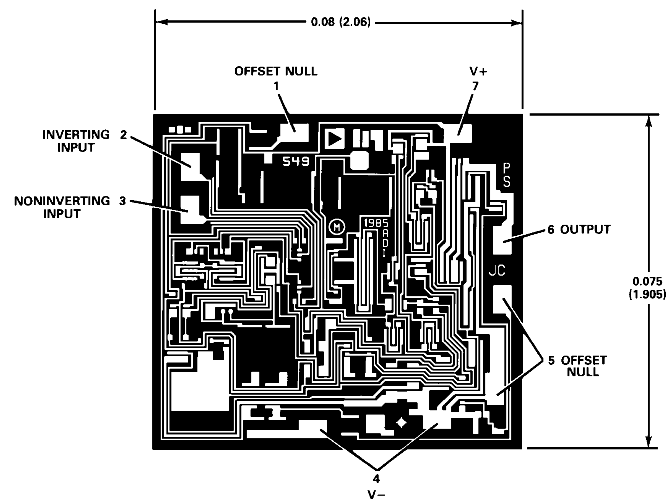
ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . ±18 V
Internal Power Dissipation . . . . 500 mW
Input Voltage . . . . ±18 V[2]
Output Short Circuit Duration . . . . Indefinite
Differential Input Voltage . . . . $+V_S$ and $-V_S$
Storage Temperature Range (H) . . . . –65°C to +125°C
Operating Temperature Range
AD549J (K, L) . . . . 0°C to +70°C
AD549S . . . . –55°C to +125°C
Lead Temperature Range (Soldering 60 sec) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD549 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



AD549–Typical Characteristics

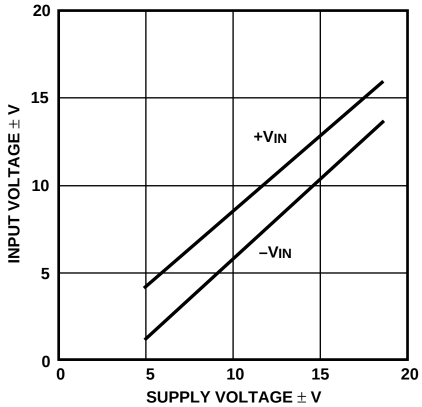


Figure 1. Input Voltage Range vs. Supply Voltage

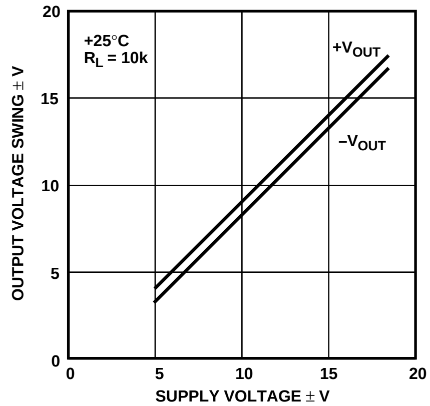


Figure 2. Output Voltage Swing vs. Supply Voltage

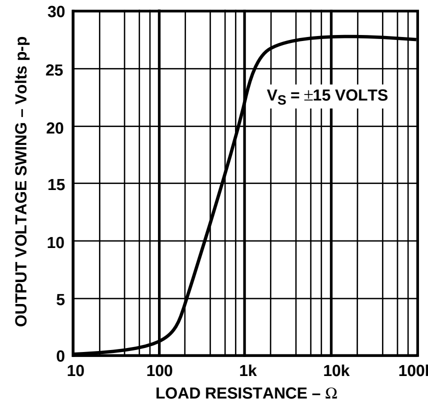


Figure 3. Output Voltage Swing vs. Load Resistance

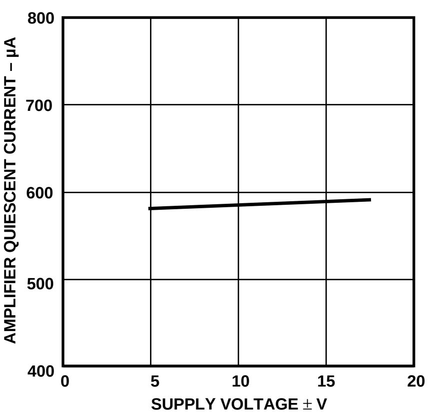


Figure 4. Quiescent Current vs. Supply Voltage

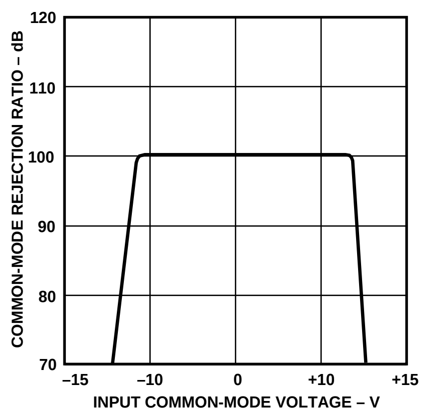


Figure 5. CMRR vs. Input Common-Mode Voltage

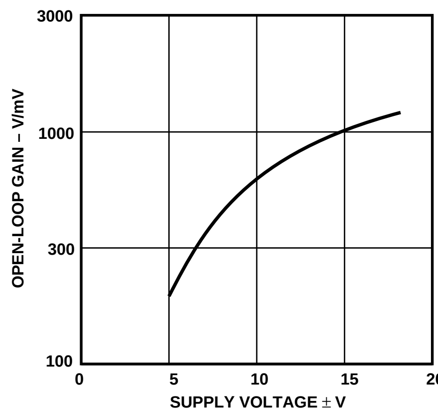


Figure 6. Open-Loop Gain vs. Supply Voltage

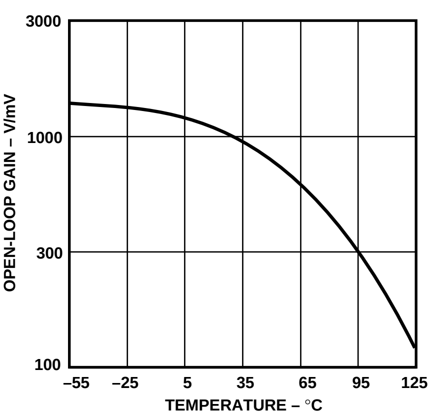


Figure 7. Open-Loop Gain vs. Temperature

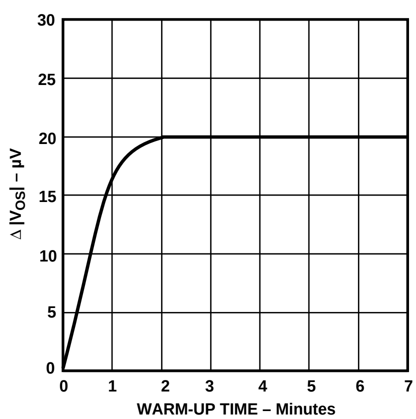


Figure 8. Change in Offset Voltage vs. Warm-Up Time

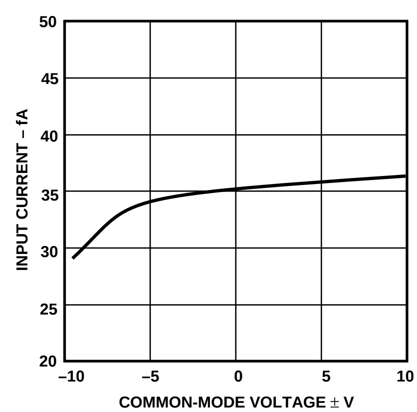


Figure 9. Input Bias Current vs. Common-Mode Voltage

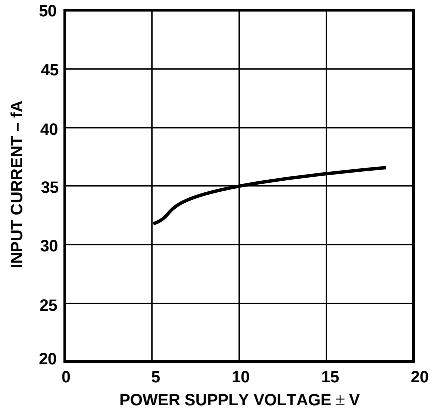


Figure 10. Input Bias Current vs. Supply Voltage

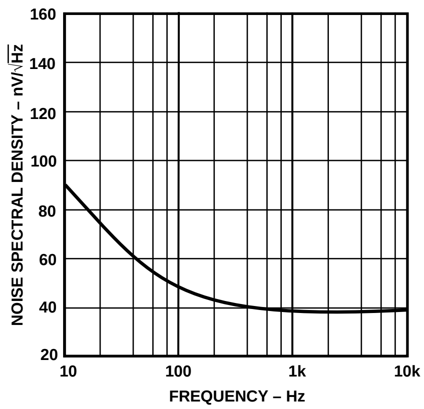


Figure 11. Input Voltage Noise Spectral Density

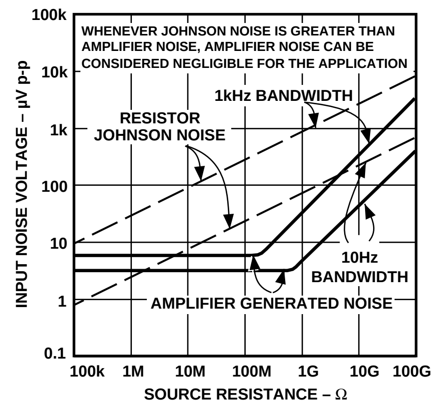


Figure 12. Noise vs. Source Resistance

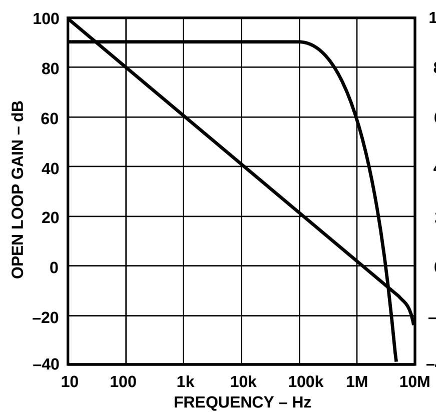


Figure 13. Open-Loop Frequency Response

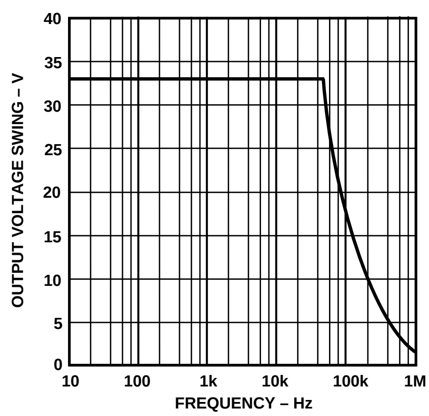


Figure 14. Large Signal Frequency Response

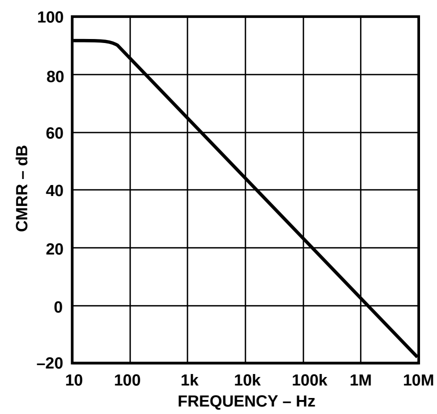


Figure 15. CMRR vs. Frequency

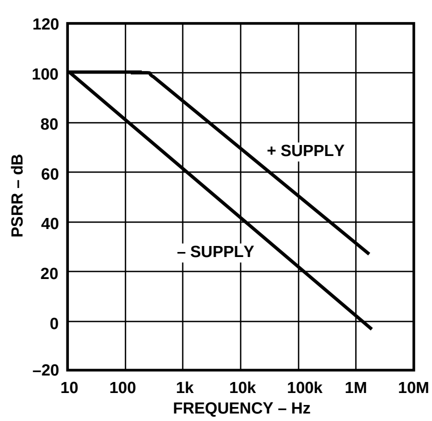


Figure 16. PSRR vs. Frequency

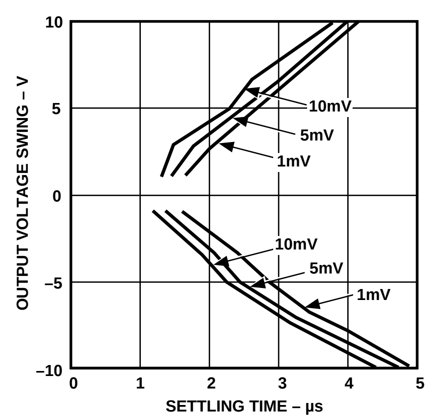


Figure 17. Output Voltage Swing and Error vs. Settling Time

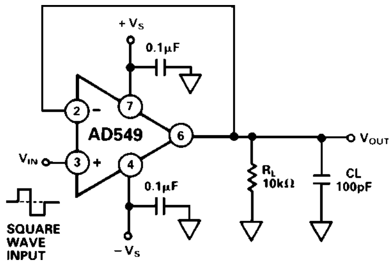


Figure 18. Unity Gain Follower

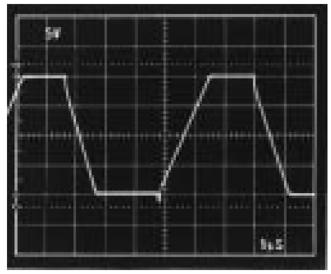


Figure 19. Unity Gain Follower Large Signal Pulse Response

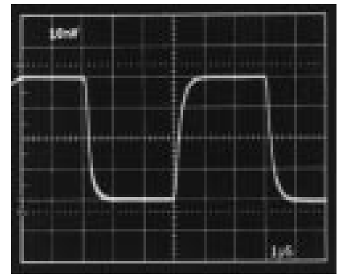


Figure 20. Unity Gain Follower Small Signal Pulse Response

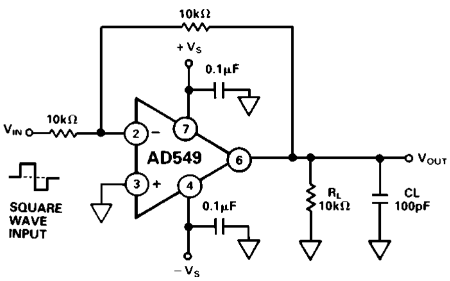


Figure 21. Unity Gain Inverter

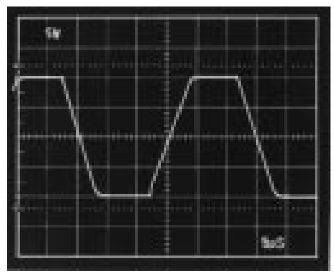


Figure 22. Unity Gain Inverter Large Signal Pulse Response

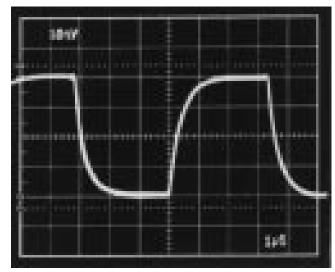


Figure 23. Unity Gain Inverter Small Signal Pulse Response

MINIMIZING INPUT CURRENT

The AD549 has been optimized for low input current and offset voltage. Careful attention to how the amplifier is used will reduce input currents in actual applications.

The amplifier operating temperature should be kept as low as possible to minimize input current. Like other JFET input amplifiers, the AD549's input current is sensitive to chip temperature, rising by a factor of 2.3 for every 10°C rise. This is illustrated in Figure 24, a plot of AD549 input current versus ambient temperature.

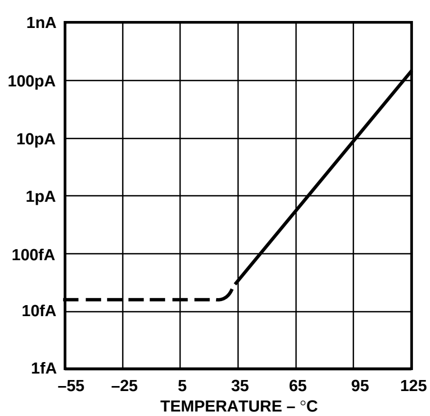


Figure 24. AD549 Input Bias Current vs. Ambient Temperature

On-chip power dissipation will raise chip operating temperature causing an increase in input bias current. Due to the AD549's low quiescent supply current, chip temperature when the (unloaded) amplifier is operated with 15 V supplies, is less than 3°C higher than ambient. The difference in input current is negligible.

However, heavy output loads can cause a significant increase in chip temperature and a corresponding increase in input current. Maintaining a minimum load resistance of 10 Ω is recommended. Input current versus additional power dissipation due to output drive current is plotted in Figure 25.

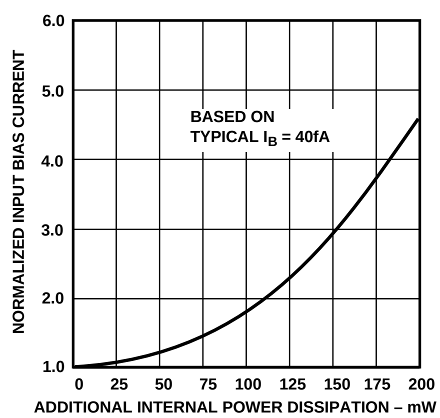


Figure 25. AD549 Input Bias Current vs. Additional Power Dissipation

CIRCUIT BOARD NOTES

There are a number of physical phenomena that generate spurious currents that degrade the accuracy of low current measurements. Figure 26 is a schematic of an I-to-V converter with these parasitic currents modeled.

Finite resistance from input lines to voltages on the board, modeled by resistor R_P, results in parasitic leakage. Insulation resistance of over 10^{15} Ω must be maintained between the amplifier's signal and supply lines in order to capitalize on the AD549's low input currents. Standard PC board material

does not have high enough insulation resistance. Therefore, the AD549's input leads should be connected to standoffs made of insulating material with adequate volume resistivity (e.g., Teflon*). The surface of the insulator's surface must be kept clean in order to preserve surface resistivity. For Teflon, an effective cleaning procedure consists of swabbing the surface with high-grade isopropyl alcohol, rinsing with deionized water, and baking the board at 80°C for 10 minutes.

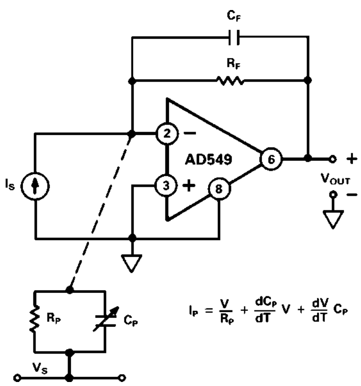


Figure 26. Sources of Parasitic Leakage Currents

In addition to high volume and surface resistivity, other properties are desirable in the insulating material chosen. Resistance to water absorption is important since surface water films drastically reduce surface resistivity. The insulator chosen should also exhibit minimal piezoelectric effects (charge emission due to mechanical stress) and triboelectric effects (charge generated by friction). Charge imbalances generated by these mechanisms can appear as parasitic leakage currents. These effects are modeled by variable capacitor C_P in Figure 26. The table in Figure 27 lists various insulators and their properties.[1]

Material	Volume Resistivity (Ω–CM)	Minimal Triboelectric Effects	Minimal Piezoelectric Effects	Resistance to Water Absorption
Teflon*	10^{17}–10^{18}	W	W	G
Kel-F**	10^{17}–10^{18}	W	M	G
Sapphire	10^{16}–10^{18}	M	G	G
Polyethylene	10^{14}–10^{18}	M	G	M
Polystyrene	10^{12}–10^{18}	W	M	M
Ceramic	10^{12}–10^{14}	W	M	W
Glass Epoxy	10^{10}–10^{17}	W	M	W
PVC	10^{10}–10^{15}	G	M	G
Phenolic	10^{5}–10^{12}	W	G	W

G–Good with Regard to Property
M–Moderate with Regard to Property
W–Weak with Regard to Property

Figure 27. Insulating Materials and Characteristics

Guarding the input lines by completely surrounding them with a metal conductor biased near the input lines' potential has two major benefits. First, parasitic leakage from the signal line is reduced since the voltage between the input line and the guard is very low. Second, stray capacitance at the input node is minimized. Input capacitance can substantially degrade signal bandwidth and the stability of the I-to-V converter. The case of the AD549 is connected to Pin 8 so that it can be bootstrapped near the input potential. This minimizes pin leakage and input common-mode capacitance due to the case. Guard schemes for inverting and noninverting amplifier topologies are illustrated in Figures 28 and 29.

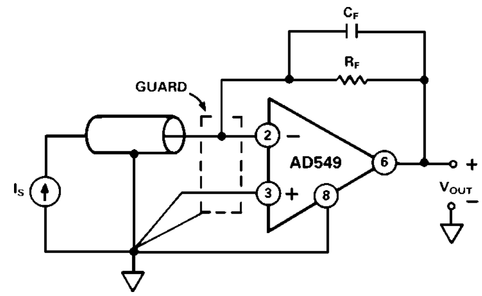


Figure 28. Inverting Amplifier with Guard

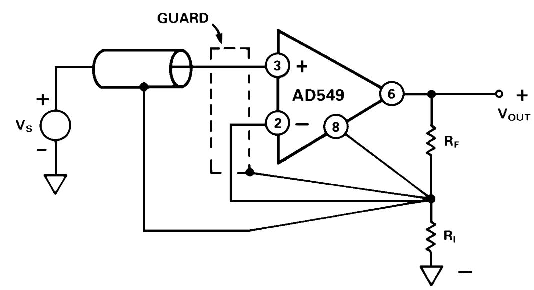


Figure 29. Noninverting Amplifier with Guard

Other guidelines include keeping the circuit layout as compact as possible and input lines short. Keeping the assembly rigid and minimizing sources of vibration will reduce triboelectric and piezoelectric effects. All precision high impedance circuitry requires shielding against interference noise. Low noise coax or triax cables should be used for remote connections to the input signal lines.

OFFSET NULLING

The AD549's input offset voltage can be nulled by using balance Pins 1 and 5, as shown in Figure 30. Nulling the input offset voltage in this fashion will introduce an added input offset voltage drift component of 2.4 μV/°C per millivolt of nulled offset (a maximum additional drift of 0.6 μV/°C for the AD549K, 1.2 μV/°C for the AD549L, 2.4 μV/°C for the AD549J).

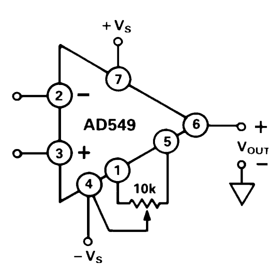


Figure 30. Standard Offset Null Circuit

The approach in Figure 31 can be used when the amplifier is used as an inverter. This method introduces a small voltage referenced to the power supplies in series with the amplifier's

[1]Electronic Measurements, pp. 15–17, Keithley Instruments, Inc., Cleveland, Ohio, 1977.
*Teflon is a registered trademark of E.I. DuPont Co.
**Kel-F is a registered trademark of 3-M Company.

positive input terminal. The amplifier's input offset voltage drift with temperature is not affected. However, variation of the power supply voltages will cause offset shifts.

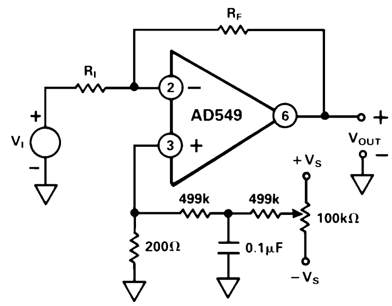


Figure 31. Alternate Offset Null Circuit for Inverter

AC RESPONSE WITH HIGH VALUE SOURCE AND FEEDBACK RESISTANCE

Source and feedback resistances greater than 100 kΩ will magnify the effect of input capacitances (stray and inherent to the AD549) on the ac behavior of the circuit. The effects of common-mode and differential input capacitances should be taken into account since the circuit's bandwidth and stability can be adversely affected.

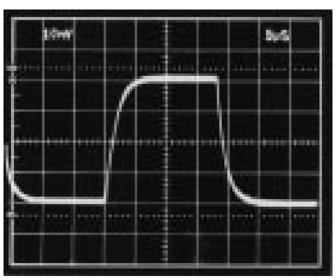


Figure 32. Follower Pulse Response from 1 MΩ Source Resistance, Case Not Bootstrapped

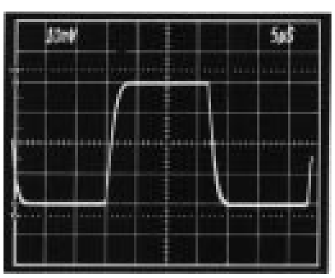


Figure 33. Follower Pulse Response from 1 MΩ Source Resistance, Case Bootstrapped

In a follower, the source resistance and input common-mode capacitance form a pole that limits the bandwidth to 1/2 π R_SC_S. Bootstrapping the metal case by connecting Pin 8 to the output minimizes capacitance due to the package. Figures 32 and 33 show the follower pulse response from a 1 MΩ source resistance with and without the package connected to the output. Typical common-mode input capacitance for the AD549 is 0.8 pF.

In an inverting configuration, the differential input capacitance forms a pole in the circuit's loop transmission. This can create peaking in the ac response and possible instability. A feedback capacitance can be used to stabilize the circuit. The inverter pulse response with R_F and R_S equal to 1 MΩ appears in Figure 34. Figure 35 shows the response of the same circuit with a I pF feedback capacitance. Typical differential input capacitance for the AD549 is 1 pF.

COMMON-MODE INPUT VOLTAGE OVERLOAD

The rated common-mode input voltage range of the AD549 is from 3 V less than the positive supply voltage to 5 V greater than the negative supply voltage. Exceeding this range will degrade the amplifier's CMRR. Driving the common-mode voltage above the positive supply will cause the amplifier's output to saturate at the upper limit of output voltage. Recovery time is typically 2 μs after the input has been returned to within the normal operating range. Driving the input common-mode voltage within 1 V of the negative supply causes phase reversal of the output signal. In this case, normal operation is typically resumed within 0.5 μs of the input voltage returning within range.

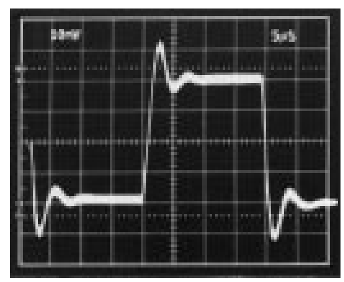


Figure 34. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance

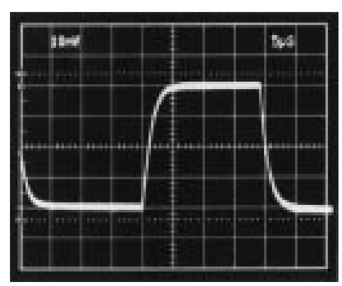


Figure 35. Inverter Pulse Response with 1 MΩ Source and Feedback Resistance, 1 pF Feedback Capacitance

DIFFERENTIAL INPUT VOLTAGE OVERLOAD

A plot of the AD549's input currents versus differential input voltage (defined as $V_{IN}+ - V_{IN}-$) appears in Figure 36. The input current at either terminal stays below a few hundred femtoamps until one input terminal is forced higher than 1 V to 1.5 V above the other terminal. Under these conditions, the input current limits at 30 μA.

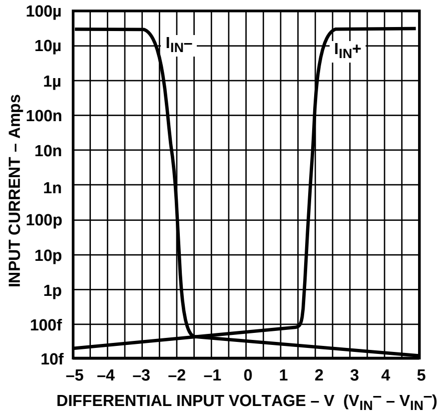


Figure 36. Input Current vs. Differential Input Voltage

INPUT PROTECTION

The AD549 safely handles any input voltage within the supply voltage range. Subjecting the input terminals to voltages beyond the power supply can destroy the device or cause shifts in input current or offset voltage if the amplifier is not protected.

A protection scheme for the amplifier as an inverter is shown in Figure 37. R_P is chosen to limit the current through the inverting input to 1 mA for expected transient (less than 1 second) overvoltage conditions, or to 100 µA for a continuous overload. Since R_P is inside the feedback loop, and is much lower in value than the amplifier's input resistance, it does not affect the inverter's dc gain. However, the Johnson noise of the resistor will add root sum of squares to the amplifier's input noise.

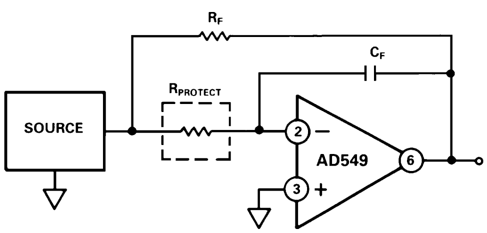


Figure 37. Inverter with Input Current Limit

In the corresponding version of this scheme for a follower, shown in Figure 38, R_P and the capacitance at the positive input terminal will produce a pole in the signal frequency response at a f = 1/2 π RC. Again, the Johnson noise R_P will add to the amplifier's input voltage noise.

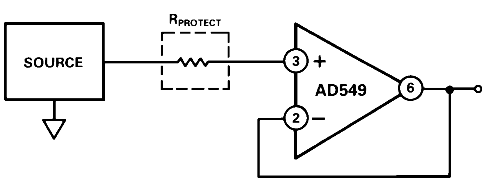


Figure 38. Follower with Input Current Limit

Figure 39 is a schematic of the AD549 as an inverter with an input voltage clamp. Bootstrapping the clamp diodes at the inverting input minimizes the voltage across the clamps and keeps the leakage due to the diodes low. Low leakage diodes, such as the FD333's should be used, and should be shielded from light to keep photocurrents from being generated. Even with these precautions, the diodes will measurably increase the input current and capacitance.

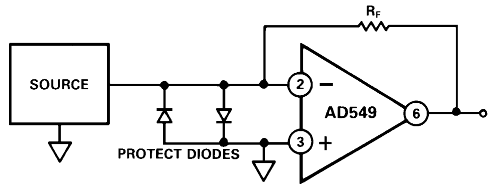


Figure 39. Input Voltage Clamp with Diodes

SAMPLE AND DIFFERENCE CIRCUIT TO MEASURE ELECTROMETER LEAKAGE CURRENTS

There are a number of methods used to test electrometer leakage currents, including current integration and direct current to voltage conversion. Regardless of the method used, board and interconnect cleanliness, proper choice of insulating materials (such as Teflon or Kel-F), correct guarding and shielding techniques and care in physi-cal layout are essential to making accurate leakage measurements.

Figure 40 is a schematic of the sample and difference circuit. It uses two AD549 electrometer amplifiers (A and B) as current-to voltage converters with high value (10^{10} Ω) sense resistors (RSa and RSb). R1 and R2 provide for an overall circuit sensitivity of 10 fA/mV (10 pA full scale). C_C and C_F provide noise suppression and loop compensation. C_C should be a low leakage polystyrene capacitor. An ultralow leakage Kel-F test socket is used for contacting the device under test. Rigid Teflon coaxial cable is used to make connections to all high impedance nodes. The

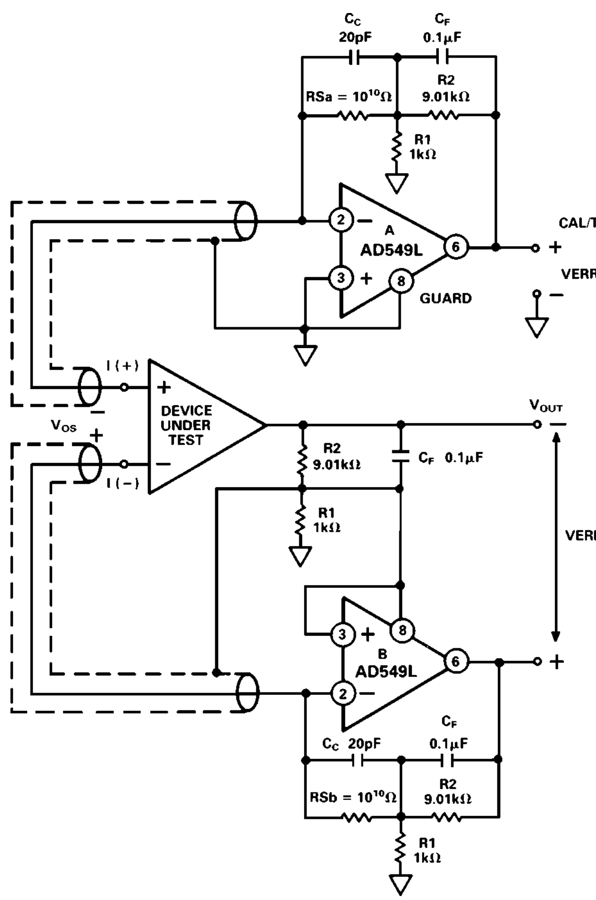


Figure 40. Sample and Difference Circuit for Measuring Electrometer Leakage Currents

use of rigid coax affords immunity to error induced by mechanical vibration and provides an outer conductor for shielding. The entire circuit is enclosed in a grounded metal box.

The test apparatus is calibrated without a device under test present. A five minute stabilization period after the power is turned on is required. First, V_{ERR1} and V_{ERR2} are measured. These voltages are the errors caused by offset voltages and leakage currents of the current to voltage converters.

$$V_{ERR1} = 10\ (V_{OS}A - I_BA \times RSa)$$

$$V_{ERR2} = 10\ (V_{OS}B - I_BB \times RSb)$$

Once measured, these errors are subtracted from the readings taken with a device under test present. Amplifier B closes the feedback loop to the device under test, in addition to providing current to voltage conversion. The offset error of the device under test appears as a common-mode signal and does not affect the test measurement. As a result, only the leakage current of the device under test is measured.

$$V_A - V_{ERR1} = 10[RSa \times I_B(+)]$$

$$V_X - V_{ERR2} = 10[RSb \times I_B(-)]$$

Although a series of devices can be tested after only one calibration measurement, calibration should be updated periodically to compensate for any thermal drift of the current to voltage converters or changes in the ambient environment. Laboratory results have shown that repeatable measurements within 10 fA can be realized when this apparatus is properly implemented. These results are achieved in part by the design of the circuit, which eliminates relays and other parasitic leakage paths in the high impedance signal lines, and in part by the inherent cancellation of errors through the calibration and measurement procedure.

PHOTODIODE INTERFACE

The AD549's low input current and low input offset voltage make it an excellent choice for very sensitive photodiode preamps (Figure 41). The photodiode develops a signal current, I_S equal to:

$$I_S = R \times P$$

where P is light power incident on the diode's surface in Watts and R is the photodiode responsivity in Amps/Watt. R_F converts the signal current to an output voltage:

$$V_{OUT} = R_F \times I_S$$

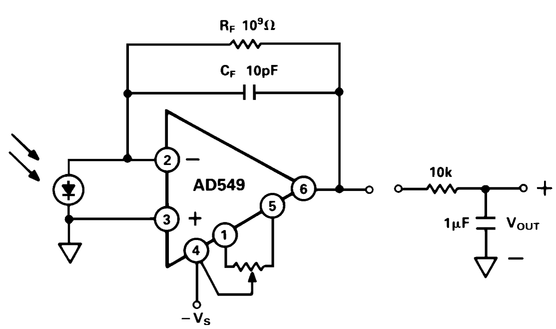


Figure 41. Photodiode Preamp

DC error sources and an equivalent circuit for a small area (0.2 mm square) photodiode are indicated in Figure 42.

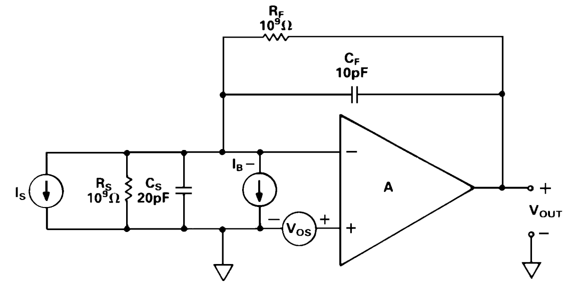


Figure 42. Photodiode Preamp DC Error Sources

Input current, I_B, will contribute an output voltage error, V_{E1}, proportional to the feedback resistance:

$$V_{E1} = I_B \times R_F$$

The op amp's input voltage offset will cause an error current through the photodiode's shunt resistance, R_S:

$$I = V_{OS}/R_S$$

The error current will result in an error voltage (V_{E2}) at the amplifier's output equal to:

$$V_{E2} = (\ I + R_F/R_S)\ V_{OS}$$

Given typical values of photodiode shunt resistance (on the order of 10^9 Ω), R_F/R_S can easily be greater than one, especially if a large feedback resistance is used. Also, R_F/R_S will increase with temperature, as photodiode shunt resistance typically drops by a factor of two for every 10°C rise in temperature. An op amp with low offset voltage and low drift must be used in order to maintain accuracy. The AD549K offers guaranteed maximum 0.25 mV offset voltage, and 5 mV/°C drift for very sensitive applications.

Photodiode Preamp Noise

Noise limits the signal resolution obtainable with the preamp. The output voltage noise divided by the feedback resistance is the minimum current signal that can be detected. This minimum detectable current divided by the responsivity of the photodiode represents the lowest light power that can be detected by the preamp.

Noise sources associated with the photodiode, amplifier, and feedback resistance are shown in Figure 43; Figure 44 is the spectral density versus frequency plot of each of the noise source's contribution to the output voltage noise (circuit parameters in Figure 42 are assumed). Each noise source's rms contribution to the total output voltage noise is obtained by integrating the square of its spectral density function over frequency. The rms value of the output voltage noise is the square root of the sum of all contributions. Minimizing the total area under these curves will optimize the preamplifier's resolution for a given bandwidth.

The photodiode preamp in Figure 41 can detect a signal current of 26 fA rms at a bandwidth of 16 Hz, which assuming a photodiode responsivity of 0.5 A/W, translates to a 52 fW rms minimum detectable power. The photodiode used has a high source resistance and low junction capacitance. C_F sets the signal bandwidth with R_F and also limits the "peak" in the noise gain that multiplies the op amp's input voltage noise contribution. A single pole filter at the amplifier's output limits the op amp's output voltage noise bandwidth to 26 Hz, a frequency comparable to the signal bandwidth. This greatly improves the preamplifier's signal to noise ratio (in this case, by a factor of three).

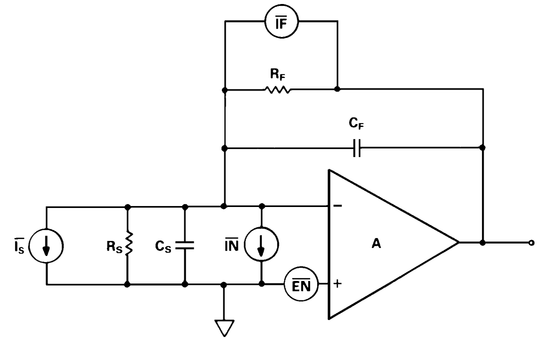


Figure 43. Photodiode Preamp Noise Sources

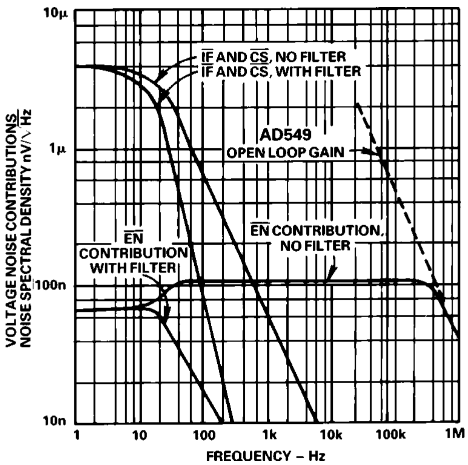


Figure 44. Photodiode Preamp Noise Sources' Spectral Density vs. Frequency

Log Ratio Amplifier

Logarithmic ratio circuits are useful for processing signals with wide dynamic range. The AD549L's 60 fA maximum input current makes it possible to build a log ratio amplifier with 1% log conformance for input current ranging from 10 pA to 1 mA, a dynamic range of 160 dB.

The log ratio amplifier in Figure 45 provides an output voltage proportional to the log base 10 of the ratio of the input currents I1 and I2. Resistors R1 and R2 are provided for voltage inputs. Since NPN devices are used in the feedback loop of the front-end amplifiers that provide the log transfer function, the output is valid only for positive input voltages and input currents. The input currents set the collector currents IC1 and IC2 of a matched pair of log transistors Q1 and Q2 to develop voltages VA and VB:

$$VA, B = -(kT/q)\ ln\ IC/IES$$

where IES is the transistors' saturation current.

The difference of VA and VB is taken by the subtractor section to obtain:

$$VC = (kT/q)\ ln\ (IC2/IC1)$$

VC is scaled up by the ratio of (R9 + R10)/R8, which is equal to approximately 16 at room temperature, resulting in the output voltage:

$$V_{OUT} = 1 \times log\ (IC2/IC1)\ V.$$

R8 is a resistor with a positive 3500 ppm/°C temperature coefficient to provide the necessary temperature compensation. The parallel combination of R15 and R7 is provided to keep the subtracter section's gain for positive and negative inputs matched over temperature.

Frequency compensation is provided by R11, R12, and C1 and C2. The bandwidth of the circuit is 300 kHz at input signals greater than 50 µA, and decreases smoothly with decreasing signal levels.

To trim the circuit, set the input currents to 10 µA and trim A3's offset using the amplifier's trim potentiometer so the output equals 0. Then set I1 to 1 µA and adjust the output to equal 1 V by trimming R10. Additional offset trims on the amplifiers A1 and A2 can be used to increase the voltage input accuracy and dynamic range.

The very low input current of the AD549 makes this circuit useful over a very wide range of signal currents. The total input current (which determines the low level accuracy of the circuit) is the sum of the amplifier input current, the leakage across the compensating capacitor (negligible if polystyrene or Teflon capacitor is used), and the collector to collector, and collector to base leakages of one side of the dual log transistors. The magnitude of these last two leakages depend on the amplifier's input offset voltage and are typically less than 10 fA with 1 mV offsets. The low level accuracy is limited primarily by the amplifier's input current, only 60 fA maximum when the AD549L is used.

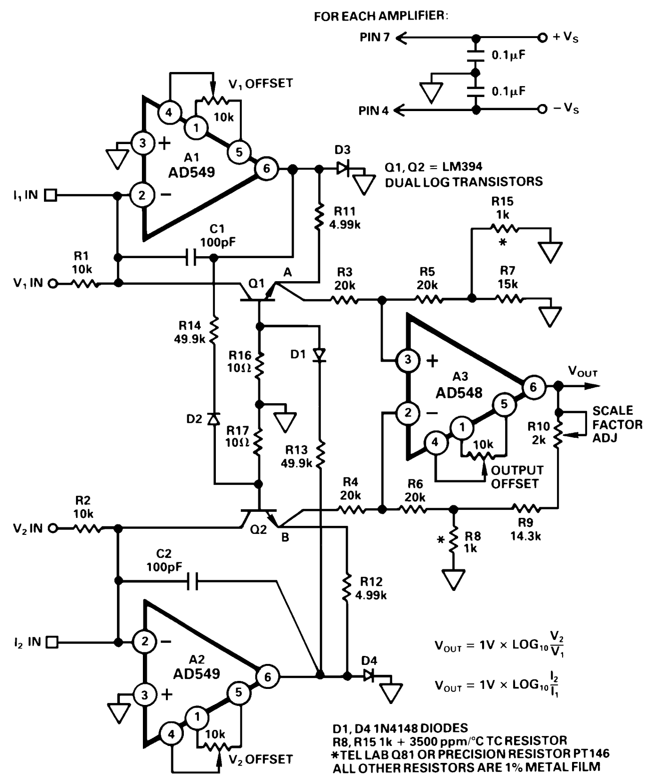


Figure 45. Log Ratio Amplifier

The effects of the emitter resistance of Q1 and Q2 can degrade the circuit's accuracy at input currents above 100 µA. The networks composed of R13, D1, R16, and R14, D2, R17 compensate for these errors, so that this circuit has less than 1% log conformance error at 1 mA input currents. The correct value for R13 and R14 depends on the type of log transistors used. 49.9 kΩ resistors were chosen for use with LM394 transistors. Smaller resistance values will be needed for smaller log transistors.

TEMPERATURE COMPENSATED pH PROBE AMPLIFIER

A pH probe can be modeled as a mV-level voltage source with a series source resistance dependent upon the electrode's composition and configuration. The glass bulb resistance of a typical pH electrode pair falls between 10^6 and 10^9 Ω. It is therefore important to select an amplifier with low enough input currents such that the voltage drop produced by the amplifier's input bias current and the electrode resistance does not become an appreciable percentage of a pH unit.

The circuit in Figure 46 illustrates the use of the AD549 as a pH probe amplifier. As with other electrometer applications, the use of guarding, shielding, Teflon standoffs, etc., is a must in order to capitalize on the AD549's low input current. If an AD549L (60 fA max input current) is used, the error contributed by input current will be held below 60 µV for pH electrode source impedances up to 10^9 Ω. Input offset voltage (which can be trimmed) will be below 0.5 mV.

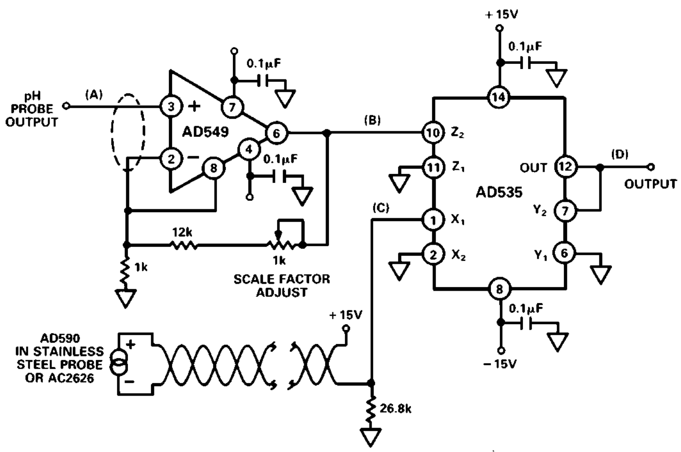


Figure 46. Temperature Compensated pH Probe Amplifier

The pH probe output is ideally zero volts at a pH of 7 independent of temperature. The slope of the probe's transfer function, though predictable, is temperature dependent (–54.2 mV/pH at 0 and –74.04 mV/pH at 100°C). By using an AD590 temperature sensor and an AD535 analog divider, an accurate temperature compensation network can be added to the basic pH probe amplifier. The table in Figure 47 shows voltages at various points and illustrates the compensation. The AD549 is set for a noninverting gain of 13.51. The output of the AD590 circuitry (point C) will be equal to 10 V at 100°C and decrease by 26.8 mV/°C. The output of the AD535 analog divider (point D) will be a temperature compensated output voltage centered at zero volts for a pH of 7, and having a transfer function of –1.00 V/pH unit. The output range spans from –7.00 V (pH = 14) to +7.00 V (pH = 0).

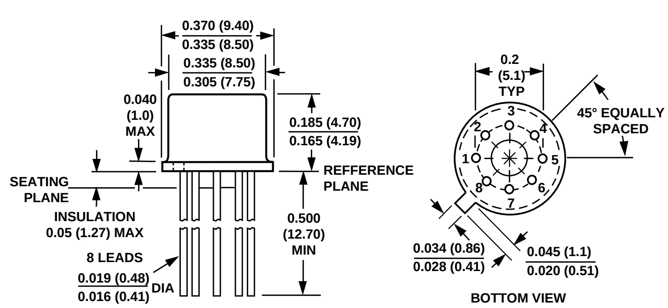
PROBE TEMP	A (PROBE OUTPUT)	B (A × 13.51)	C (590 OUTPUT)	D (10 B/C)
0	54.20 mV	0.732 V	7.32 V	1.00 V
25°C	59.16 mV	0.799 V	7.99 V	1.00 V
37°C	61.54 mV	0.831 V	8.31 V	1.00 V
60°C	66.10 mV	0.893 V	8.93 V	1.00 V
100°C	74.04 mV	1.000 V	10.00 V	1.00 V

Figure 47. Table Illustrating Temperature Compensation

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

TO-99 (H) Package



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